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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/689,946	10/21/2003	Robert H. Bishop	5646-98	4031

7590 10/20/2004

EXAMINER	
PAREKH, NITIN	

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ART UNIT	PAPER NUMBER
2811	

DATE MAILED: 10/20/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)
	10/689,946	Bishop, et al.
	Examiner	Art Unit
	Nitin Parekh	2811

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *21 October 2003*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-25* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-25* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *21 October 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date 2.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 112

1. The following is a quotation of the first paragraph of 35 U.S.C. 112:

> The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

2. Claims 1 and 7 are rejected under 35 U.S.C. 112, first paragraph, as failing to comply with the enablement requirement. The claim(s) contains subject matter which was not described in the specification in such a way as to enable one skilled in the art to which it pertains, or with which it is most nearly connected, to make and/or use the invention.

A. The limitations as recited in claim 1, line 6, include "a routing channel in the array that increases the periphery of the array by at least four external connectors compared to absence of the routing channel".

However, the specification and figures describe the following:

1. Fig. 1A: The number of external peripheral connectors along the periphery without any routing channel (RC) is 12 and those in presence of the RC is 11, therefore, the RC reduces the external peripheral connectors by 1.

2. Fig. 4: The number of external peripheral connectors along the periphery without any routing channel (RC) is 16 and those in presence of the RC is 15, therefore, the RC reduces the external peripheral connectors by 1.

Therefore, it is not clear from the specification how the peripheral connectors/external connectors in the periphery are increased by 4 by incorporating the RC.

B. The limitations as recited in claim 7, line 2 include "Cp, of the array" and "Cp > or = 2N + 2M".

However, it is not clear what is the Cp, whether it is a number of external connector in the peripheral rows, peripheral columns, a total number of those in peripheral rows and columns or a total number of those surrounding the routing channel.

Claim Rejections - 35 USC § 102

3. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> **A person shall be entitled to a patent unless –**
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

4. Claims 1-3, 8-10 and 20-22, insofar as being in compliance with 35 U.S.C. 112, are rejected under 35 U.S.C. 102(b) as being anticipated by Iwasaki (US Pat. 5814890).

Regarding claims 1-3, Iwasaki discloses a grid array microelectronic package comprising:

- a circuit board substrate/first substrate (CBS-7 in Fig. 3-5)
- an array/first array of external connectors (10 in Fig. 3-5) on the substrate that are arranged in a plurality of rows and columns to define a periphery of the array along outer two rows and two columns towards edges of the CBS and an interior of the array, the external connectors being in a form of flat pad/bump (see 10 in Fig. 3)
- a variety of configurations of the external connectors including areas/routing channels having missing external connectors (see Fig. 6-13) where the area/routing channel reduces a number of external peripheral connectors along the periphery (rows and columns) by 12 (see Fig. 7 v/s 5), 14 (see Fig. 8 v/s 5), etc. when compared to those in the periphery in absence of the routing channel (Fig. 5), and
- the configurations comprising the arrays including 25 missing connectors (see Fig. 6), 31 missing connectors (see Fig. 7), etc.

(Fig. 3-13; Col. 4, line 65- Col. 7, line 58).

Regarding claims 8-10, Iwasaki teaches the entire claimed structure as applied to claim 1 above, wherein Iwasaki further teaches:

- the variety of configurations of the external connectors having five rows and eleven columns (see Fig. 7-13), including a pair of peripheral rows and a pair of peripheral columns at a periphery thereof and pairs of interior rows and interior columns between the respective pair of peripheral rows and peripheral columns
- wherein an external connector in the peripheral column and one external connector in an interior column adjacent thereto are missing (see two or more missing connectors from the peripheral columns in the configurations of Fig. 7-13) from the array to define a routing channel that extends from the periphery of the array towards the interior of the array, and
- a first external connector in a peripheral column, a second external connector in a first interior row adjacent the peripheral column and a third external connector in a third interior column adjacent the first interior column and remote from the peripheral column are missing (see three missing connectors from the peripheral columns in the configurations of Fig. 7, 8, 10 and 11) from the array to define the routing channel that extends from the periphery of the array towards the interior of the array.

Regarding claims 20-22, Iwasaki teaches the entire claimed structure as applied to claims 1 and 8 above, wherein Iwasaki further teaches the external connectors being dummy/operationally disconnected, such dummy/operationally disconnected connectors can be arranged at the corners or in the routing channels at a desired pattern/arrangement outside the lattice of the external connectors (see 9 in Fig. 8 and 10; Col. 7, lines 30-58). Furthermore, such routing channels can include two or three adjacent dummy/operationally disconnected connectors in the area having missing connectors in the peripheral columns and the adjacent interior columns and extending from the periphery of the array towards the interior of the array (see Fig. 8 and 10).

Claim Rejections - 35 USC § 103

5. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> **(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.**

6. Claims 4, 11 and 23, insofar as being in compliance with 35 U.S.C. 112, are rejected under 35 U.S.C. 103(a) as being unpatentable over Iwasaki (US Pat. 5814890) in view of Iwasaki (US Pat. 5773882).

Regarding claims 4, 11 and 23, Iwasaki teaches substantially the entire claimed structure as applied to claims 1, 8 and 20 above, except a plurality of signal conductors that extend along the routing channel.

Iwasaki ('882 patent) teaches using a substrate having external connection pads/bumps (see 6a in Fig. 2) where a wiring lines/signal connector lines (see 6b in Fig. 2) are incorporated as routing channels in an area of missing external connection pads/bumps to provide the desire electrical routing and interconnection (Col. 3, lines 10-42).

It would have been obvious to a person of ordinary skill in the art at the time invention was made to incorporate the plurality of signal conductors that extend along the routing channel as taught by Iwasaki ('882 patent) so that the wiring interconnection density can be increased and the desired circuit routing can be achieved in Iwasaki's grid array package (GAP).

7. Claims 5, 6, 12-16, 18, 19, 24 and 25, insofar as being in compliance with 35 U.S.C. 112, are rejected under 35 U.S.C. 103(a) as being unpatentable over Iwasaki (US Pat. 5814890) in view of Dockerty et al. (US Pat. 5796169).

Regarding claims 5, 6, 12, 13, 24 and 25, Iwasaki teaches substantially the entire claimed structure as applied to claims 1, 8 and 20 above, except the package further comprising:

- a second substrate, and
- a second array of external connectors on the second substrate that are arranged to mate with the first array of external connectors.

Dockerty et al. teach a ball grid array (BGA) package having a first substrate (see printed circuit board 1 in Fig. 1 and 2) and a second substrate (see an integrated circuit device 3 in Fig. 1 and 2) having respective first and second arrays comprising external solder ball/bump connectors (see 11 in Fig. 1-3) where the second array of external connectors on the second substrate are bonded/mated with the respective first array of external connectors to provide the desired interconnection (Fig. 1-3; Col. 3 and 4)

It would have been obvious to a person of ordinary skill in the art at the time invention was made to incorporate the second substrate and the second array of external connectors on the second substrate being arranged to mate with the first array of external connectors as taught by Dockerty et al. so that the desired interconnection and circuit routing between the two substrates can be achieved in Iwasaki's GAP.

Regarding claims 14-16, Iwasaki teaches substantially the entire claimed structure as applied to claims 1 and 8 above, except at least one external connector in a peripheral row or peripheral column and at least one external connector in an interior row or interior column adjacent thereto are electrically strapped together to define a routing channel that extends from the periphery of the array towards the interior of the array.

Dockerty et al. teach the BGA package having the external solder ball/bump connectors (see SBC 11 in Fig. 1-4) where the SBC are electrically connected/strapped in a variety of connecting patterns having support solder (see 16 in Fig. 3) to provide the desired electrical and thermal conduction (Col. 4, line 35- Col. 5, line 25), such patterns defining the routing channels including those that extend from the periphery of the array towards the interior of the array.

It would have been obvious to a person of ordinary skill in the art at the time invention was made to incorporate at least one external connector in a peripheral row or peripheral column and at least one external connector in an interior row or interior column adjacent thereto are electrically strapped together to define a routing channel that extends from the periphery of the array towards the interior of the array as taught by Dockerty et al. so that the desired electrical/thermal conduction and circuit routing can be achieved in Iwasaki's GAP.

Regarding claims 18 and 19, Iwasaki and Dockerty et al. teach substantially the entire claimed structure as applied to claims 14, 1, 5 and 6 above.

8. Claim 17, insofar as being in compliance with 35 U.S.C. 112, is rejected under 35 U.S.C. 103(a) as being unpatentable over Iwasaki (US Pat. 5814890) and Dockerty et al. (US Pat. 5796169) as applied to claim 14 above, and further in view of Iwasaki (US Pat. 5773882).

Regarding claim 17, Iwasaki, Dockerty et al. and Iwasaki ('882 patent) teach substantially the entire claimed structure as applied to claims 14, 1, and 4 above.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Nitin Parekh whose telephone number is 571-272-1663. The examiner can normally be reached on 09:00AM-05:30PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Eddie Lee can be reached on 571-272-1732. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9318.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is 703-308-0956.

Nitin Parekh

NP

NITIN PAREKH

10-13-04

PATENT EXAMINER

Technology Center 2800